Amendment to Claims

This listing of Claims will replace all prior versions and listings of claims in this Application.

Listing of Claims

Claim 1. (CURRENTLY AMENDED) A method of forming a substrate for use in ~~IC~~ CMOS device fabrication comprising:

preparing a silicon substrate, including doping a bulk silicon (100) substrate with ions taken from the group of ions to form a doped substrate taken from the group of doped substrates consisting of n-type doped substrates and p-type doped substrates;

forming a first relaxed SiGe layer on the silicon substrate;

forming a first tensile-strained silicon cap on the first relaxed SiGe layer;

forming a second relaxed SiGe layer on the first tensile-strained silicon cap;

forming a second tensile-strained silicon cap on the second relaxed SiGe layer; and

completing ~~an IC device~~ a CMOS device on the tensile-strained silicon cap, wherein the CMOS device includes a source region and a drain region which are both in electrical contact with a tensile-strained silicon cap, including well ion implantation, threshold voltage adjustment, STI device isolation, gate oxidation, gate electrode and sidewall nitride formation; etching of gate oxide after formation of sidewall nitride; etching of exposed second tensile-strained silicon cap to expose second relaxed SiGe layer in the source region and the drain region; selectively laterally etching of any SiGe layer at the source and drain region and selectively laterally etching of any SiGe layer located beneath the gate and nitride spacers, forming a resulting tunnel, which is left empty or filled with a dielectric.

Claim 2. CANCELLED

Claim 3. (CURRENTLY AMENDED) The method of claim 1 wherein said forming a first relaxed SiGe layer on the silicon substrate includes forming a graded, relaxed SiGe layer to a thickness of between about 200 nm to 5 μm, and containing between about ~~10% and 100% Ge, and preferably between about~~ 20% to 30% Ge.

Claim 4. (ORIGINAL) The method of claim 1 wherein said forming a first tensile-strained silicon cap includes forming a tensile-strained silicon cap to a thickness of between about 10 nm to 50 nm.

Claim 5. (ORIGINAL) The method of claim 1 wherein said forming a second relaxed SiGe layer on the silicon substrate includes forming a relaxed SiGe layer to a thickness of between about 25 nm to 300 nm.

Claim 6. (ORIGINAL) The method of claim 1 wherein said forming a second tensile-strained silicon cap includes forming a second tensile-strained silicon cap having a thickness of between about 10 nm to 50 nm.

Claim 7. (CURRENTLY AMENDED) A method of forming a substrate for use in CMOS fabrication comprising:

preparing a silicon substrate, including doping a bulk silicon (100) substrate with

ions taken from the group of ions to form a doped substrate taken from the group of doped substrates consisting of n-type doped substrates and p-type doped substrates;

forming a first relaxed SiGe layer on the silicon substrate;

forming a first tensile-strained silicon cap on the first relaxed SiGe layer; and

completing a CMOS device on the tensile-strained silicon cap, wherein the CMOS device includes a source region and a drain region which are both in electrical contact with a tensile-strained silicon cap, including well ion implantation, threshold voltage adjustment, STI device isolation, gate oxidation, gate electrode and sidewall nitride formation; etching of gate oxide after formation of sidewall nitride; etching of exposed second tensile-strained silicon cap to expose second relaxed SiGe layer in the source region and the drain region; selectively laterally etching of any SiGe layer at the source and drain region and selectively laterally etching of any SiGe layer located beneath the gate and nitride spacers, forming a resulting tunnel, which is left empty or filled with a dielectric.

Claim 8. (ORIGINAL) The method of claim 7 wherein said forming a first relaxed SiGe layer on the silicon substrate includes forming a relaxed SiGe layer to a thickness of between about 200 nm to 5 μm.

Claim 9. (CURRENTLY AMENDED) The method of claim 7 wherein said forming a first relaxed SiGe layer on the silicon substrate includes forming a graded relaxed SiGe layer, containing between about ~~10% and 100% Ge, and preferably between about~~ 20% to 30% Ge.

Claim 10. (ORIGINAL) The method of claim 7 wherein said forming a first tensile-strained silicon cap includes forming a tensile-strained silicon cap to a thickness of between about 10 nm to 50 nm.

Claim 11. (ORIGINAL) The method of claim 7 which includes forming a second relaxed SiGe layer on the first tensile-strained silicon cap and forming a second tensile-strained silicon cap on the second relaxed SiGe layer.

Claim 12. (ORIGINAL) The method of claim 11 wherein said forming a second relaxed SiGe layer on the silicon substrate includes forming a relaxed SiGe layer to a thickness of between about 25 nm to 300 nm.

Claim 13. (ORIGINAL) The method of claim 11 wherein said forming a second tensile-strained silicon cap includes forming a second tensile-strained silicon cap having a thickness of between about 10 nm to 50 nm.

Claim 14. CANCELLED

Claim 15. CANCELLED

Claim 16. (CURRENTLY AMENDED) A method of forming a substrate for use in CMOS fabrication comprising:

preparing a silicon substrate, including doping a bulk silicon (100) substrate with ions taken from the group of ions to form a doped substrate taken from the group of doped substrates consisting of n-type doped substrates and p-type doped substrates;

forming a first relaxed SiGe layer on the silicon substrate, including forming a graded, relaxed SiGe layer to a thickness of between about 200 nm to 5 μm, and containing between about 10% and 100% Ge, and preferably between about 20% to 30% Ge;

forming a first tensile-strained silicon cap on the first relaxed SiGe layer having a thickness of between about 10 nm to 50 nm; and

completing a CMOS device on the tensile-strained silicon cap, wherein the CMOS device includes a source region and a drain region which are both in electrical contact with a tensile-strained silicon cap, including well ion implantation, threshold voltage adjustment, STI device isolation, gate oxidation, gate electrode and sidewall nitride formation; etching of gate oxide after formation of sidewall nitride; etching of exposed second tensile-strained silicon cap to expose second relaxed SiGe layer in the source region and the drain region; selectively laterally etching of any SiGe layer at the source and drain region and selectively laterally etching of any SiGe layer located beneath the gate and nitride spacers, forming a resulting tunnel, which is left empty or filled with a dielectric.

Claim 17. (ORIGINAL) The method of claim 16 which includes forming a second relaxed SiGe layer on the first tensile-strained silicon cap and forming a second tensile-strained silicon cap on the second relaxed SiGe layer.

Claim 18. (ORIGINAL) The method of claim 17 wherein said forming a second relaxed SiGe layer on the silicon substrate includes forming a relaxed SiGe layer to a thickness of between about 25 nm to 300 nm.

Claim 19. (ORIGINAL) The method of claim 17 wherein said forming a second tensile-strained silicon cap includes forming a second tensile-strained silicon cap having a thickness of between about 10 nm to 50 nm.

Claim 20. CANCELLED

Claim 21. CANCELLED